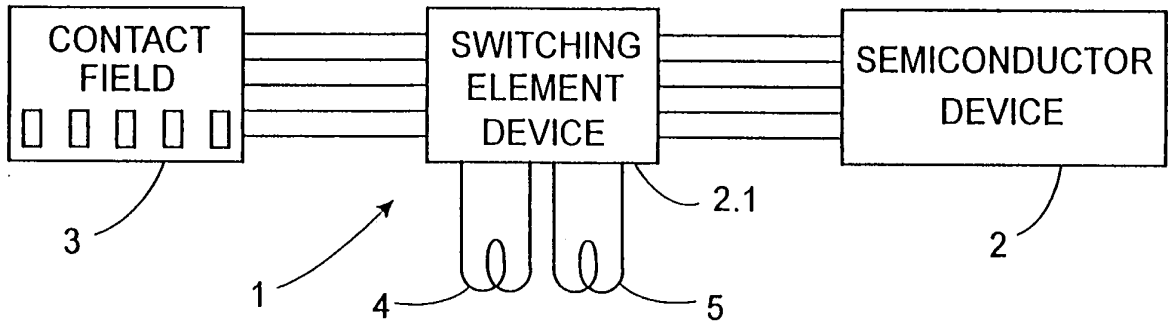

Fig. 1 (PRIOR ART)

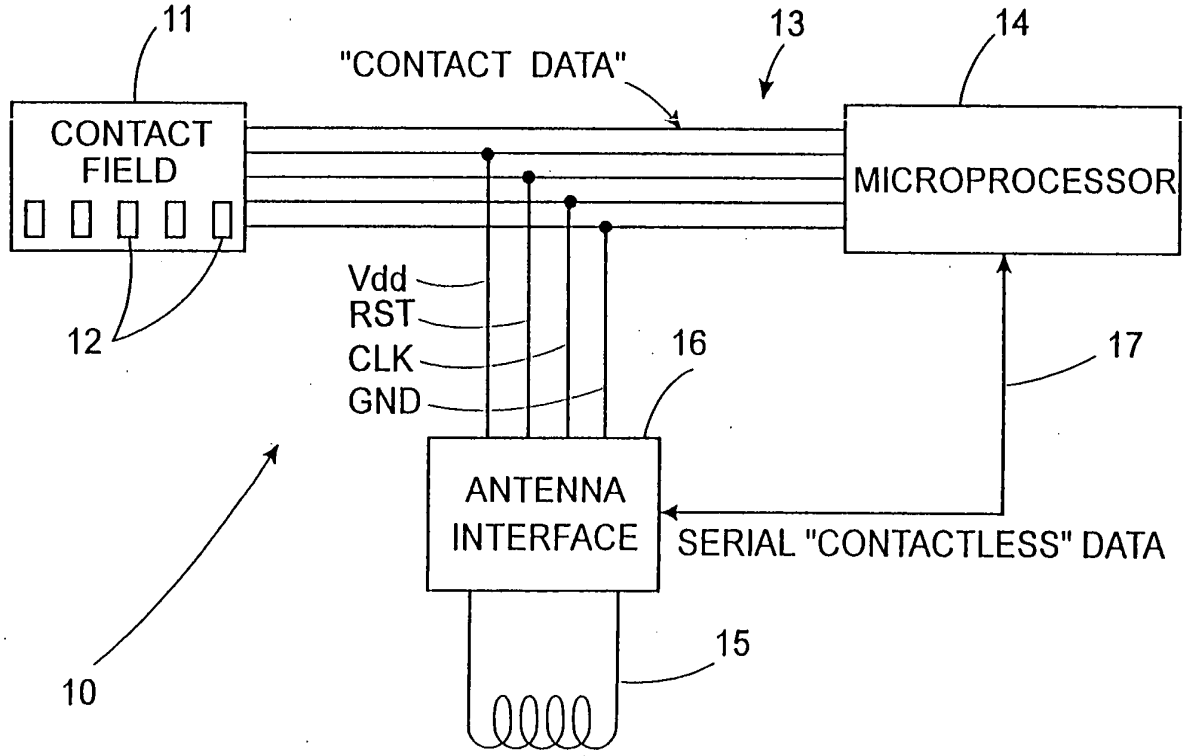

Fig. 2

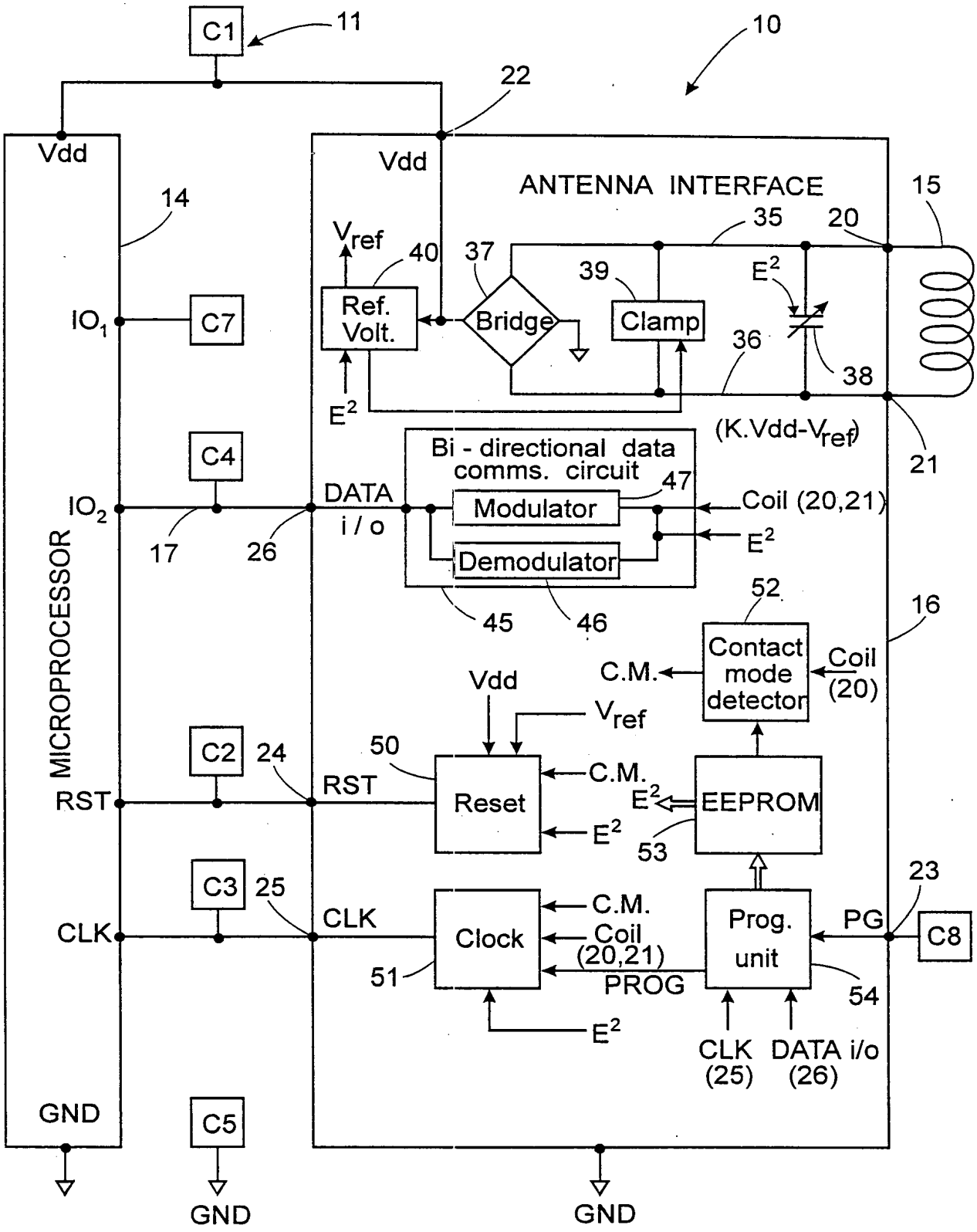
C1
11
10
22
Vdd
Vdd
ANTENNA INTERFACE
15
14
35
20
V_{ref}
40
37
39
E^2
IO_1
C7
Ref. Volt.
Bridge
Clamp
36
38
E^2
$(K.Vdd-V_{ref})$
21
C4
Bi - directional data comms. circuit
47
IO_2
DATA i / o
Modulator
Coil (20,21)
E^2
17
26
Demodulator
45
46
52
16
Contact mode detector
C.M.
Coil (20)
Vdd
V_{ref}
MICROPROCESSOR
C2
24
50
C.M.
RST
RST
Reset
E^2
EEPROM
E^2
53
C3
25
23
C.M.
CLK
CLK
Clock
Coil (20,21)
Prog. unit
PG
C8
51
PROG
54
E^2
CLK (25)
DATA i/o (26)
GND
C5
GND
GND

Fig. 3

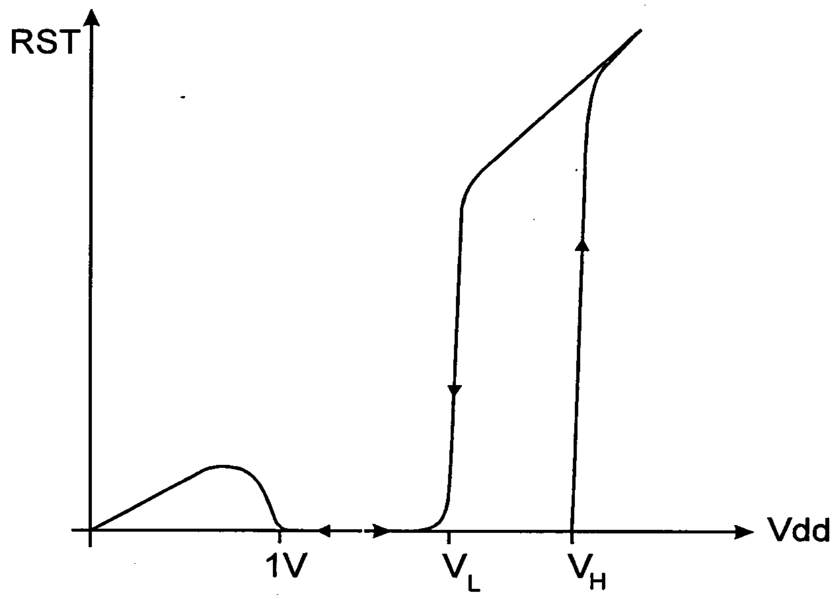

Fig. 4

MICROPROCESSOR		ANTENNA INTERFACE	
CONTACT MODE	CONTACTLESS MODE	CONTACT MODE	CONTACTLESS MODE
Vdd = ʃ RST = ʃ CLK = ЛЛЛL IO_2 = 0 ⇒ C.M DATA via IO_1 C.M { data transaction ISO 7816	Vdd = / RST = ʃ CLK = ЛЛЛL IO_2 = 1 ⇒ C / L DATA via IO_2 C/L { data transaction CONTACTLESS PROTOCOL	Vdd = ʃ RST, CLK = TRISTATE E / M FIELD OFF ⇒ C.M. MODE	Vdd = / RST = ʃ CLK = ЛЛЛL E / M FIELD ON ⇒ C/L. MODE DATA TRANSACTION via IO_2

Fig. 5

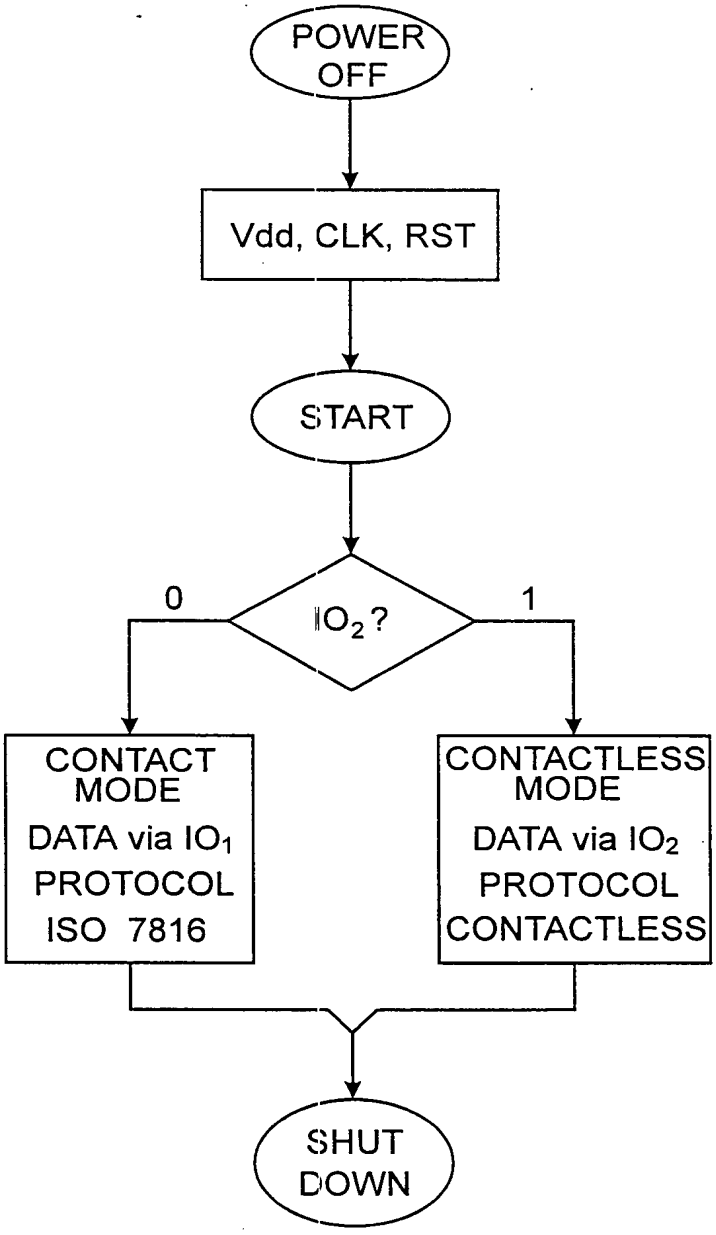
POWER OFF
Vdd, CLK, RST
START
0
IO2 ?
1
CONTACT MODE
DATA via IO1
PROTOCOL
ISO 7816
CONTACTLESS MODE
DATA via IO2
PROTOCOL
CONTACTLESS
SHUT DOWN

Fig. 6

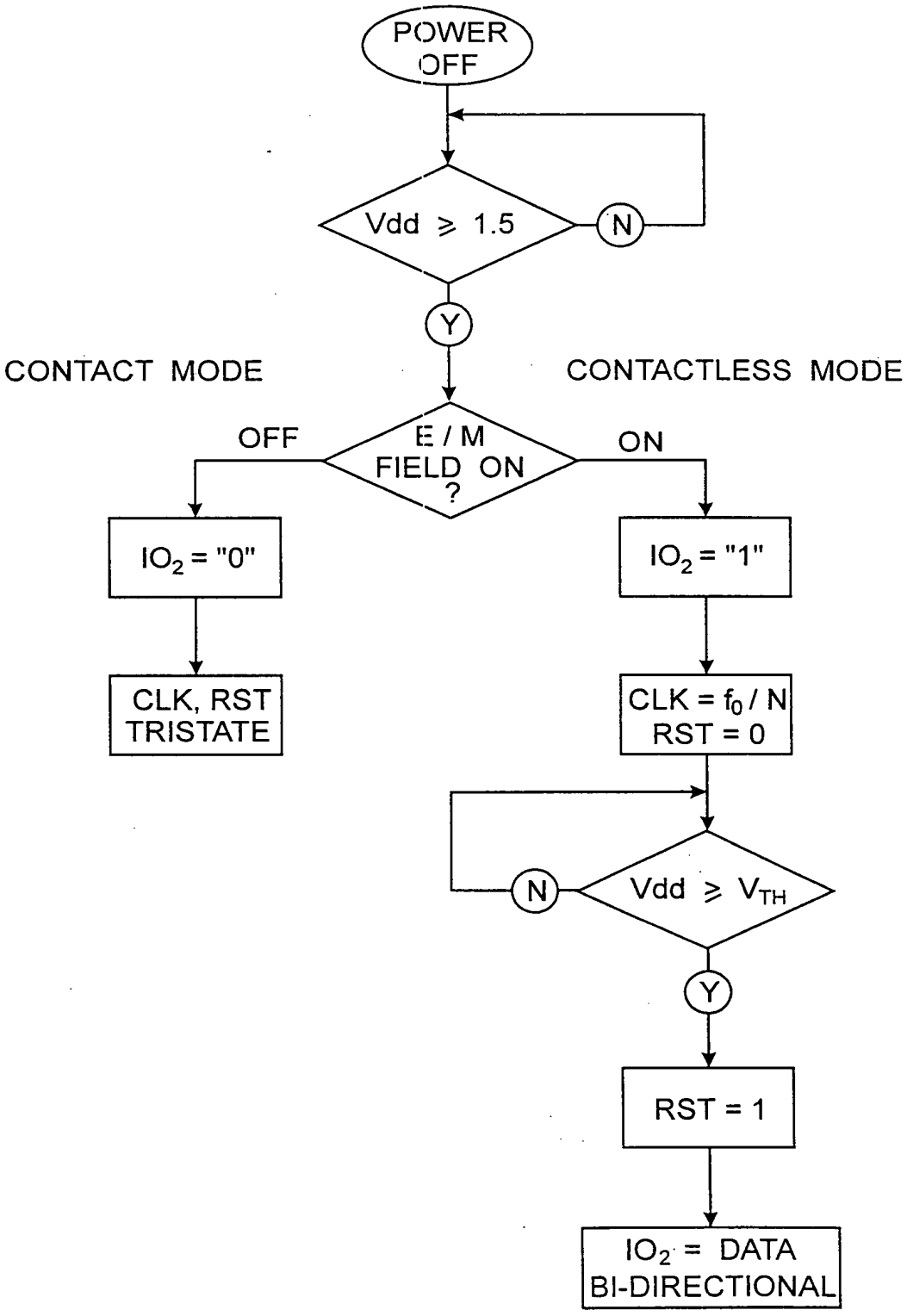
POWER OFF
Vdd ≥ 1.5
N
Y
CONTACT MODE
CONTACTLESS MODE
OFF
E / M FIELD ON ?
ON
IO2 = "0"
IO2 = "1"
CLK, RST TRISTATE
CLK = f0 / N
RST = 0
N
Vdd ≥ VTH
Y
RST = 1
IO2 = DATA BI-DIRECTIONAL

Fig. 7

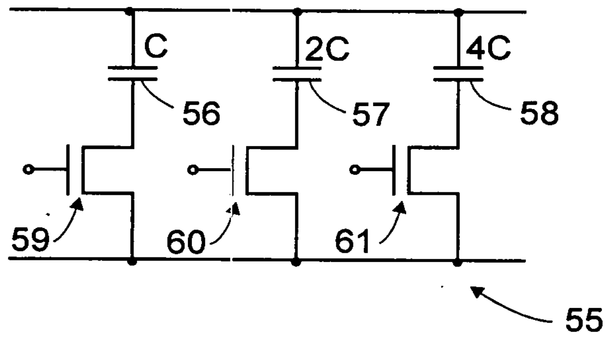

Fig. 8a

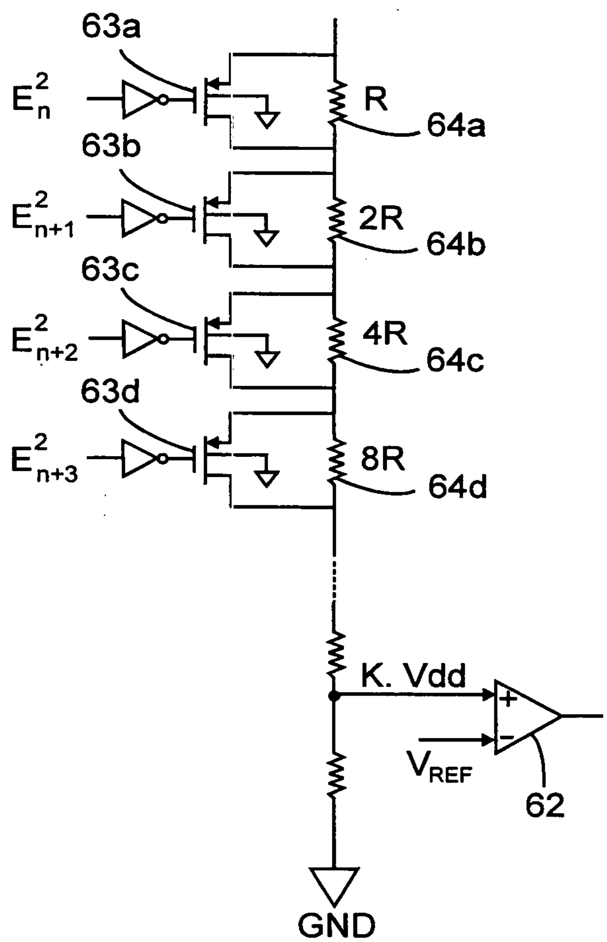

Fig. 8b

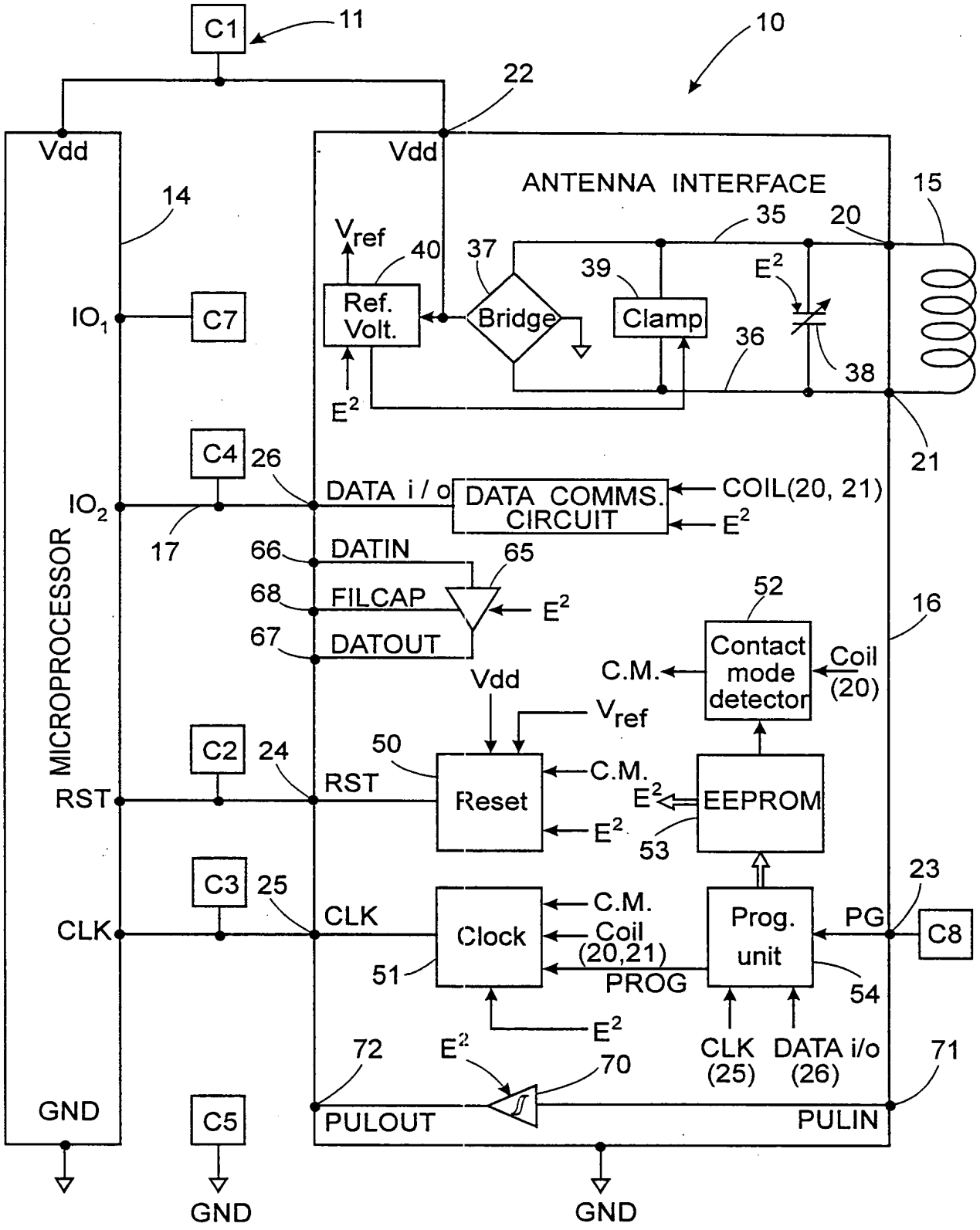
C1
11
10
22
Vdd
Vdd
ANTENNA INTERFACE
15
14
35
20
V_{ref}
40
37
39
E^2
IO_1
C7
Ref. Volt.
Bridge
Clamp
36
38
E^2
21
C4
26
IO_2
DATA i / o
DATA COMMS. CIRCUIT
COIL(20, 21)
E^2
17
66
DATIN
65
68
FILCAP
E^2
52
16
67
DATOUT
Contact mode detector
C.M.
Coil (20)
Vdd
V_{ref}
MICROPROCESSOR
C2
24
50
C.M.
RST
RST
Reset
E^2
EEPROM
E^2
53
C3
25
23
CLK
CLK
Clock
C.M.
Coil (20,21)
Prog. unit
PG
C8
51
PROG
54
E^2
72
E^2
70
CLK (25)
DATA i/o (26)
71
GND
C5
PULOUT
PULIN
GND
GND

Fig. 9

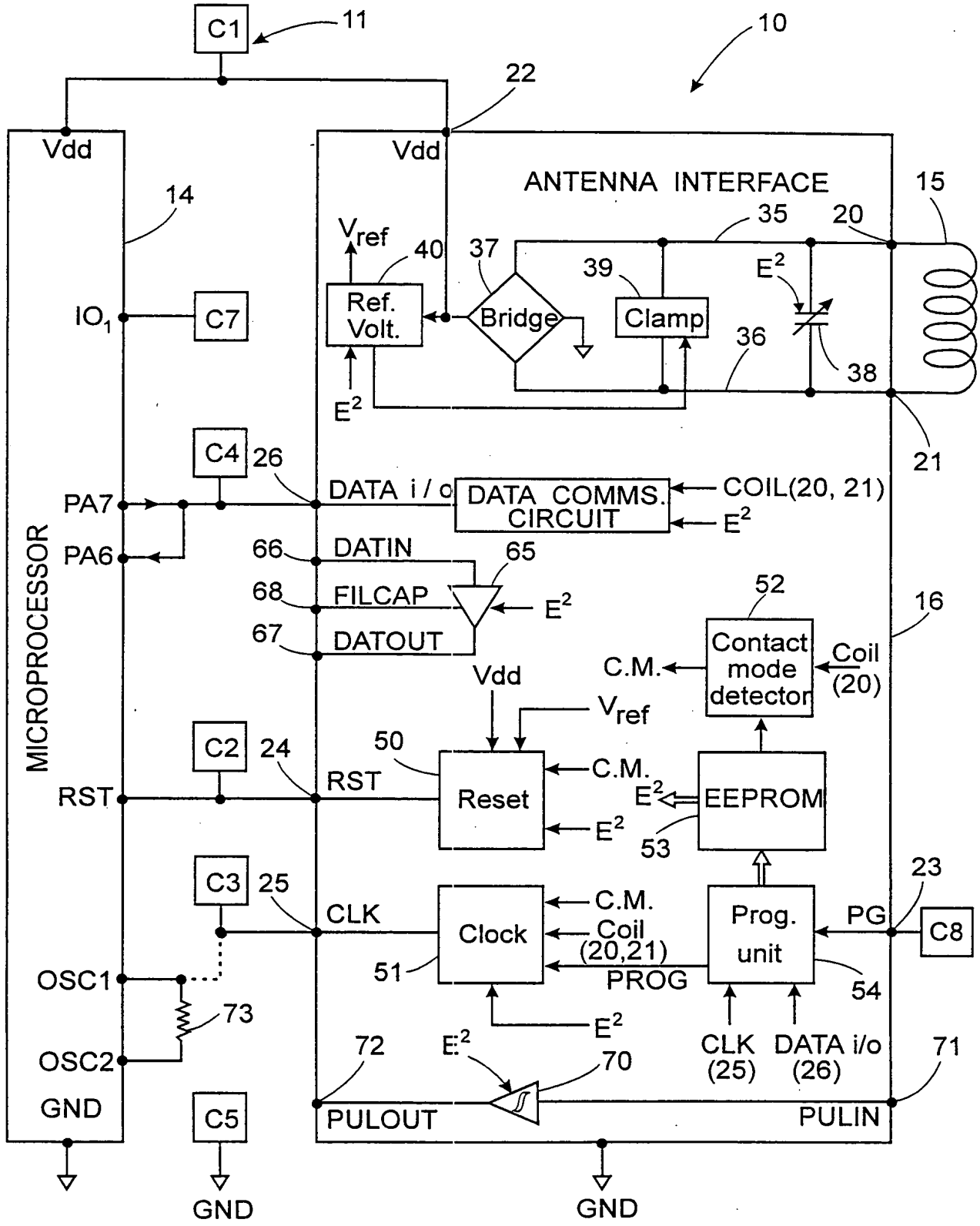
C1
11
10
22
Vdd
Vdd
ANTENNA INTERFACE
15
14
35
20
V_{ref}
40
37
39
E^2
IO_1
C7
Ref. Volt.
Bridge
Clamp
36
38
E^2
21
C4
26
PA7
DATA i / o
DATA COMMS. CIRCUIT
COIL(20, 21)
E^2
PA6
66
DATIN
65
68
FILCAP
E^2
52
16
67
DATOUT
Contact mode detector
C.M.
Coil (20)
Vdd
V_{ref}
MICROPROCESSOR
C2
24
50
C.M.
RST
RST
Reset
E^2
EEPROM
E^2
53
C3
25
23
CLK
Clock
C.M.
Coil (20,21)
Prog. unit
PG
C8
OSC1
51
PROG
54
73
E^2
OSC2
72
E^2
70
CLK (25)
DATA i/o (26)
71
GND
C5
PULOUT
PULIN
GND
GND

Fig. 10

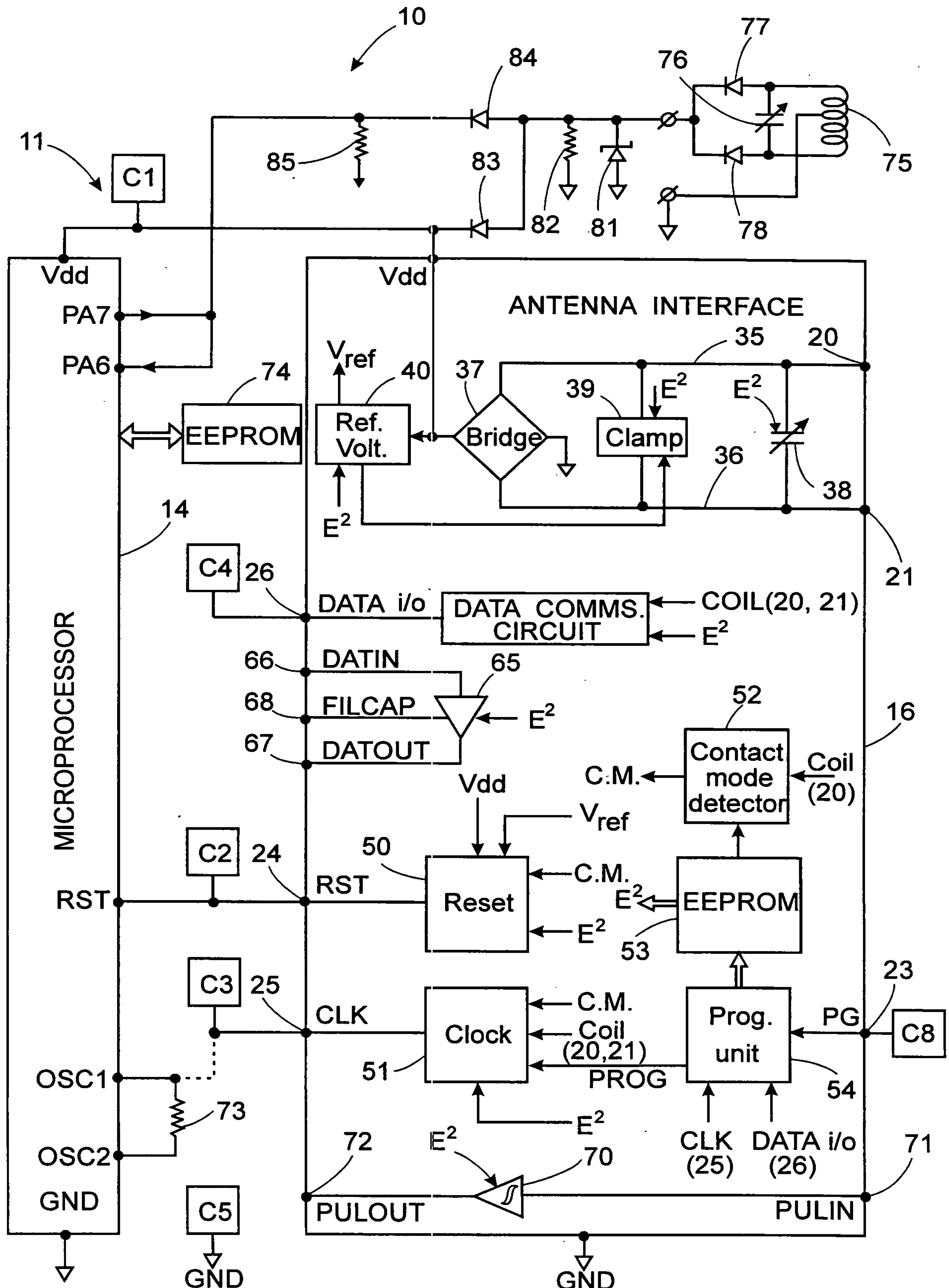
10
11
C1
84
85
83
82
81
76
77
75
78
Vdd
PA7
PA6
RST
OSC1
OSC2
GND
MICROPROCESSOR
14
74
EEPROM
Vdd
ANTENNA INTERFACE
Vref
40
Ref. Volt.
37
Bridge
39
Clamp
E2
35
20
36
38
21
C4
26
DATA i/o
DATA COMMS. CIRCUIT
COIL(20, 21)
66
DATIN
65
68
FILCAP
67
DATOUT
52
Contact mode detector
C.M.
Coil (20)
16
Vdd
Vref
C2
24
50
Reset
EEPROM
53
C3
25
CLK
Clock
51
C.M.
Coil (20,21)
PROG
Prog. unit
PG
23
C8
54
73
72
70
CLK (25)
DATA i/o (26)
71
PULOUT
PULIN
C5
GND
GND

Fig. 11

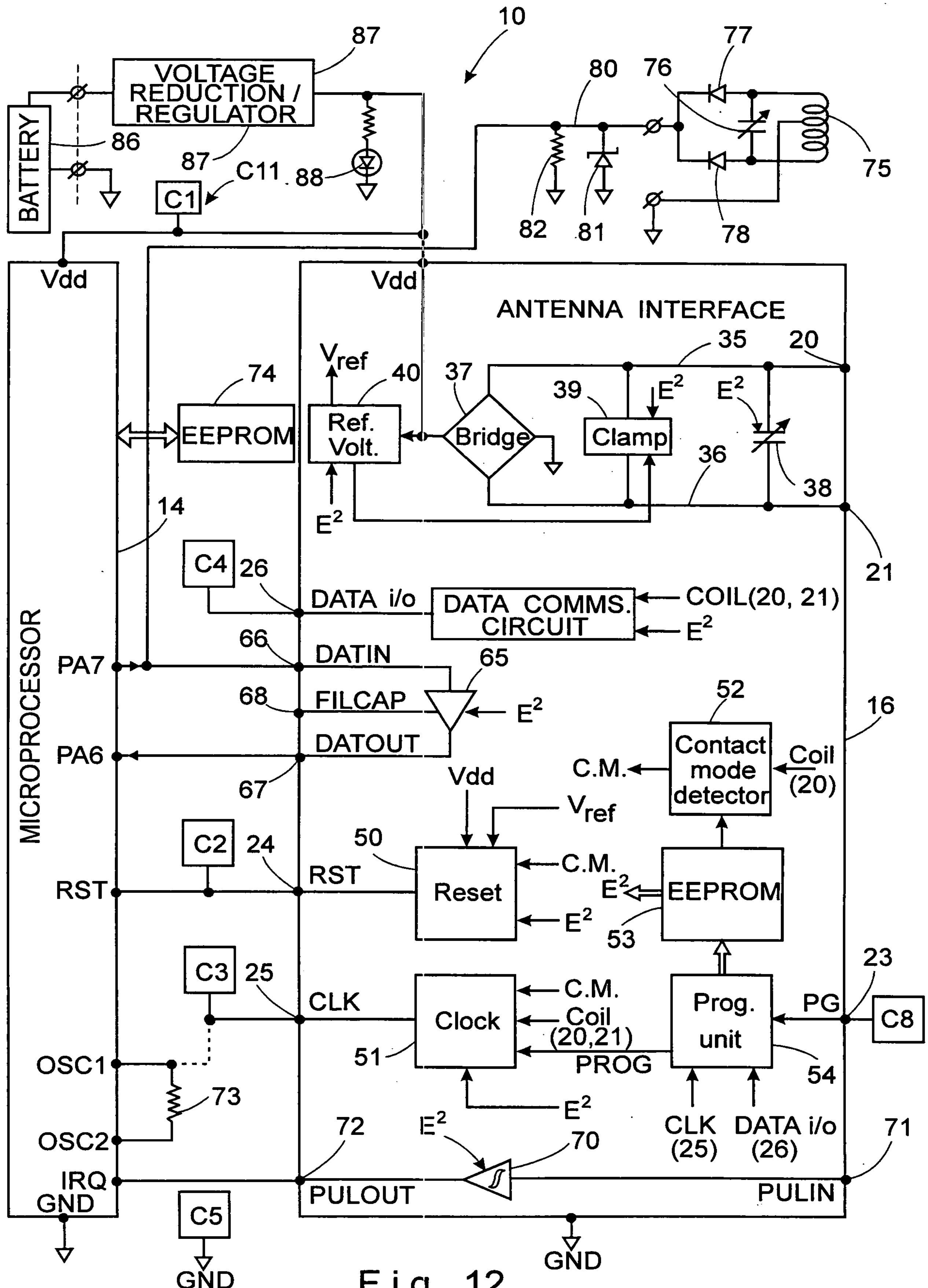
10
VOLTAGE REDUCTION / REGULATOR
BATTERY
87
86
C11
C1
88
80
76
77
75
82
81
78
Vdd
MICROPROCESSOR
ANTENNA INTERFACE
35
20
Vref
40
37
39
E2
Ref. Volt.
Bridge
Clamp
36
38
74
EEPROM
14
21
C4
26
DATA i/o
DATA COMMS. CIRCUIT
COIL(20, 21)
66
DATIN
65
PA7
68
FILCAP
DATOUT
PA6
67
52
16
Contact mode detector
C.M.
Coil (20)
C2
24
RST
50
Reset
53
C3
25
CLK
Clock
51
Coil (20,21)
PROG
Prog. unit
PG
23
C8
54
OSC1
OSC2
73
72
70
71
IRQ
GND
PULOUT
PULIN
CLK (25)
DATA i/o (26)
C5
GND

Fig. 12